UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,337	07/28/2003	John McCollum	ACT-368	6310

28661 7590 11/21/2005

SIERRA PATENT GROUP, LTD.
P O BOX 6149
STATELINE, NV 89449

EXAMINER
SOWARD, IDA M

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 11/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,337	MCCOLLUM, JOHN	
	Examiner	Art Unit	
	Ida M. Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8,9,17,18,26,27,35 and 36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8,9,17,18,26,27,35 and 36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed October 7, 2005.

Response to Amendment

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al. (5,726,477).

In regard to claim 8, Williams et al. teach a transistor 420 for an integrated circuit comprising: a p-type substrate 402; an n-type region disposed 421 over said p-type substrate 402; n-type buried layers 423A & 423B disposed at about a boundary between said substrate 402 and said n-type region 421, said buried layers 423A & 423B doped to a higher level than said n-type region 421; spaced apart p-type source and drain regions 426 & 428 disposed in said n-type region 421 forming a channel therein; a control gate 424 disposed above and insulated from said channel; and said substrate

and said n-type region each are biased (Figure 12, columns 9-10, lines 1-67 and 1-1-59, respectively).

In regard to claim 9, Williams et al. teach an isolation trench 406 & 408 disposed in the n-type region 421 and surrounding the source and drain regions 426 & 428, the isolation trench 408 & 408 extending down into the substrate 402 (Figure 12, columns 9-10, lines 1-67 and 1-1-59, respectively).

However, Williams et al. fail to teach said substrate and said n-type region and said n-type buried layers each biased such that said n-type region is fully depleted.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to also bias the n-type buried layers of the transistor structure as taught by Williams et al. so that the n-type region is fully depleted to create threshold adjustable transistors (column 2, lines 50-55).

Claims 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al. (5,726,477) as applied to claims 8-9 above, and further in view of Uchida (US 2002/0031882 A1).

Williams et al. teach all mentioned in the rejection above.

However, Williams et al. fail to teach the various regions and layers having the opposite conductivity type.

In regard to claim 26, Uchida teaches a transistor for an integrated circuit comprising: an n-type substrate 1; a p-type region 14 disposed over said n-type substrate 1; p-type buried layer 17 disposed at about a boundary between said

substrate 1 and said p-type region 14; spaced apart n-type source and drain regions disposed in said p-type region 14 forming a channel therein; a control gate 27 disposed above and insulated from said channel (Figure 5, pages 4-5, paragraphs [0053]-[0064]).

In regard to claim 27, Uchida teaches an isolation trench 2 disposed in the p-type region 14 and surrounding the source and drain regions (Figure 5, pages 4-5, paragraphs [0053]-[0064]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to also bias the n-type buried layers of the transistor structure as taught by Williams et al. with the transistor structure having opposing conductivity type of the regions and layers as taught by Uchida to reduce power consumption (page 1, paragraph [0004]).

Claims 17-18 and 35-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al. (5,726,477) and Uchida (US 2002/0031882 A1) as applied to claims 8-9 and 26-27 above, and further in view of Taniguchi et al. (US 6,617,632 B2).

Williams et al. and Uchida teach all mentioned in the rejection above.

However, Williams et al. and Uchida fail to teach a floating gate.

Taniguchi et al. teach a floating gate 4 (Figure 6, column 12, lines 12-23).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to also bias the n-type buried layers of the transistor structure as taught by Williams et al. and the transistor structure having opposing

conductivity type of the regions and layers as taught by Uchida with the transistor having a floating gate as taught by Taniguchi et al. to provide a technology capable of preventing a drain disturb phenomenon in a nonvolatile memory semiconductor device (column 3, lines 61-64).

Response to Arguments

Applicant's arguments with respect to claims 8,9,17,18,26,27,35 and 36 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to transistors for integrated circuits:

Hsu et al. (US 6,908,818 B2) Hwang (5,359,219)

Ishimaru (5,960,272) Maeda (5,471,082)

Shimizu (US 2002/0113286 A1) Shone (5,822,243)

Shum et al. (US 2005/0180215 A1) Terashima et al. (5,874,767).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-

1845. The Examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
October 27, 2005